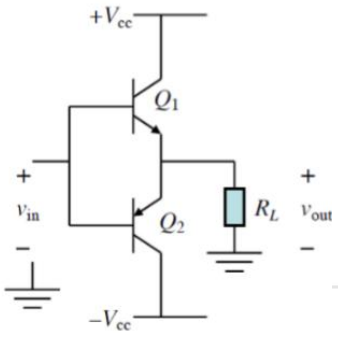


Supply current

$$I_{supply} = \frac{1}{T}\int_0^T i_{C1}dt = \frac{1}{2\pi}\int_0^{\pi} \hat{i}_{out}\sin\theta d\theta = \frac{1}{\pi}\hat{i}_{out} = \frac{1}{\pi}\frac{\hat{v}_{out}}{R_L}$$

Input power

$$P_{supply} = 2V_{cc}I_{supply} = \frac{2V_{cc}\hat{v}_{out}}{\pi R_L}$$

Output power

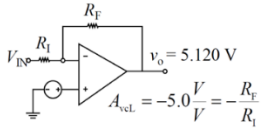
$$P_{load} = \frac{1}{2}\hat{v}_{out}\hat{i}_{out} = \frac{1}{2}\frac{\hat{v}_{out}^2}{R_L}$$

Efficiency

$$\eta = \frac{P_{load}}{P_{supply}} = \frac{\frac{1}{2}\frac{\hat{v}_{out}^2}{R_L}}{\frac{2}{\pi}\frac{V_{cc}}{R_L}\hat{v}_{out}} = \frac{\pi}{4}\frac{\hat{v}_{out}}{V_{cc}}$$

Offset: Example

An inverting feedback amplifier has a closed-loop gain of $A_{vcL} = -5$V/V. The input signal V_{IN} is -1.0 VDC. The output voltage is 5.120 VDC. What's the V_{IO} for the op-amp ?



Solution:

i) The expected output voltage is $v_o = \left(-\frac{R_F}{R_I}\right)V_{IN}$

$= -5(-1)$

$= 5.0$ VDC

ii) The actual $v_o = 5.120$ VDC

iii) The difference between (i) and (ii) is

$5.120 - 5.0 = 0.120$ VDC

iv) The input offset voltage V_{IO} will contribute to an output given by

$v_o = \left(1+\frac{R_F}{R_I}\right)V_{IO}$

$= (1+5)V_{IO}$

$= 6\ V_{IO}$

(v) The output obtained in (iv) must be 0.120 VDC.

Thus, $6V_{IO} = 120$ mV

$V_{IO} = 20$ mV

CityU

Assume that opAmp is ideal $A=\infty$

Then we get $V_f = V_-$ $I_{in} = 0$

$A_{VCL} = -\frac{R_f}{R_1} = -5 \Rightarrow R_f = 5R_1$

$\frac{V_o - V_f}{R_f} + \frac{V_{in} - V_f}{R_1} = 0$

$V_{IO} = V_f - 0V = V_f$

$V_f = V_-$ $I_{in,op\text{-}amp} = 0$

$KCL = \frac{V_{out} - V_f}{R_f} + \frac{V_{in} - V_f}{R_1} = 0$

$\frac{V_{out}}{R_f} + \frac{V_{in}}{R_1} = 0$

$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_1}$ Open loop gain $A = \frac{V_{out}}{V_{in}}$

$V_{out} = A(V_f - V_-)$

$\frac{V_o - V_{IO}}{R_f} + \frac{V_{in} - V_{IO}}{R_1} = 0$

$V_{IO}\left(R_f^{-1} + R_1^{-1}\right) = \frac{V_o}{R_f} + \frac{V_{in}}{R_1}$

$V_{IO} = \left(\frac{V_o}{R_f} + \frac{V_{in}}{R_1}\right)\left(R_f^{-1} + R_1^{-1}\right)^{-1}$

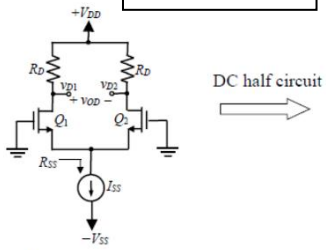
$= \left(\frac{5.12}{5R_1} + \frac{-1}{R_1}\right)\left((5R_1)^{-1} + R_1^{-1}\right)^{-1}$

$= \left(\frac{0.12}{5R_1}\right)\left(\frac{6}{5R_1}\right)^{-1}$

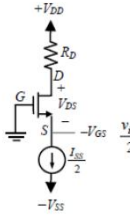
$= \left(\frac{0.12}{5R_1}\right)(5R_1) = \frac{0.12}{6} = 0.02$ V

1(a). DC Analysis

Current Mirror



DC half circuit



$I_D = \frac{I_{SS}}{2} = 150\mu A$

$V_{GS} = V_{TN} + \sqrt{\frac{2I_D}{K_n}} = 1 + \sqrt{\frac{2(1.5\times10^{-4})}{4\times10^{-4}}} = 1.866V$

$V_{DS} = 15 - (75k\Omega)I_D - (-V_{GS}) = 5.62V$

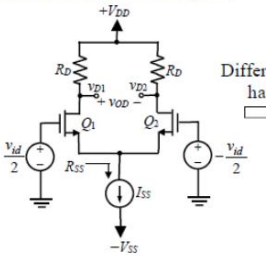
$Q\ V_{DS} = 5.62 > V_{GS} - V_{TN} = 0.866V$

Hence, the transistors are in Saturation region

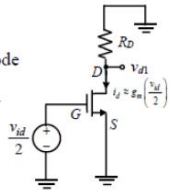
(b) AC analysis

$g_m = \sqrt{2K_nI_D} = \sqrt{2\times4\times10^{-4}\times150\mu} = 0.346mS$

Differential mode analysis:



Differential-mode half circuit



$v_{d1} = -g_m\left(\frac{v_{id}}{2}\right)R_D,\ v_{d2} = -g_m\left(-\frac{v_{id}}{2}\right)R_D$

$v_{od} = v_{d1} - v_{d2} = -g_m v_{id} R_D$

$A_{dm-diff} = \frac{v_{od}}{v_{id}} = -g_m R_D = -(0.346mS)(75k\Omega) = -26$

$A_{dm-se1} = \frac{v_{d1}}{v_{id}} = \frac{-26}{2} = -13$

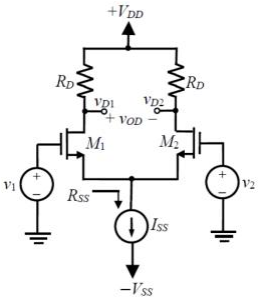
$R_{id} = \infty$

For the differential amplifier in Fig. 1, assume that the MOS transistors are ideal and Early effect can be ignored (i.e. λ=0). It is given that the single ended gain in differential mode is -5 (i.e. $A_{dm,se} = v_{D1}/v_{id} = -5$), $V_{DD} = V_{SS} = 15$ V, $R_D = 50$ kΩ, $V_{TN} = 1$V, $K_n = 100$ μA/V².

(a) What is the differential mode gain for differential output ($A_{dm,diff}$)? What is the common mode gain for differential outputs ($A_{cm,diff}$)? (Note differential output means $V_{out} = V_{D1} - V_{D2}$)

(b) What is the magnitude of I_{SS}? Draw the DC half circuit and find the Q point of the transistors.

(c) Find the CMRR for single-ended and differential outputs if $R_{SS} = 150$ kΩ.



Given $A_{dm,se} = -5$

$\frac{-g_mR_D}{2} = -5 \Rightarrow g_mR_D = 10$

$R_D = 50k\Omega$ $g_m = 0.2mS$

(i) $A_{dm,diff} = 2A_{dm,se} = -10$

$A_{cm,diff} = 0$

(ii) $g_m = \sqrt{\frac{2K_nI_{SS}}{2}}$

$I_{SS} = 400\mu A$

DC half

$V_{GS} = V_T + \sqrt{\frac{2I_{SS}}{2K_n}} = 3V$

$V_S = -V_{GS} = -3V$

$V_D = V_{DD} - I_DR_D$

$-V_{GS} = 5V$

$V_{DS} = 8V > V_{GS} - V_T$

→ saturation

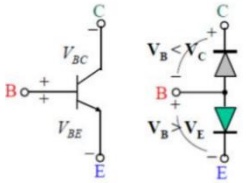
(iii) $CMRR_{diff} = \infty$

$CMRR_{se} = \frac{1+2g_mR_{SS}}{2} = 30.5$

BJT active:	Saturation:	1. Assume active.
VBE ≈ 0.7 V	VBE ≈ 0.7 V	2. Calculate IB, IC, node voltages.
IC = βIB	VCE ≈ VCE,sat	3. Check VCE > VCE,sat.
IE = (β+1)IB	IC no longer = βIB	4. If failed, redo using saturation.
VCE > VCE,sat		

Forward-active region

$I_B = I_{SS}\left(e^{V_{BE}/V_T} - 1\right)$

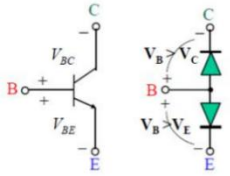


BEJ (npn) forward biased
BCJ (npn) reversed biased

$V_{BE} \approx 0.7\ \text{V}$
$I_C = \beta I_B = \alpha I_E$

⇒ **Good amplifier**

$\alpha = \beta/(\beta+1)$



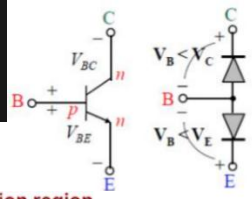
Saturation region

BEJ (npn) forward biased
BCJ (npn) forward biased

⇒ **Closed switch**

$\Rightarrow V_{BE} \approx 0.7\ \text{V}$
$V_{BC} = 0.4 \sim 0.5\ \text{V}$

$\Rightarrow V_{CE(SAT)} = 0.2 \sim 0.3\ \text{V}$



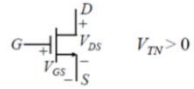
Cutoff region

BEJ (npn) reverse biased
BCJ (npn) reverse biased

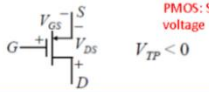
$I_C = 0$

⇒ **Open Switch**

NMOS: S is lowest voltage



$V_{TN} > 0$



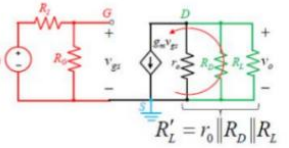
PMOS: S is highest voltage

$V_{TP} < 0$

Region	NMOS	PMOS
Cutoff	$V_{GS} < V_{TN}$ $I_D = 0$	$\lvert V_{GS}\rvert < \lvert V_{TP}\rvert$ $I_D = 0$
Triode	$V_{GS} \ge V_{TN}$ and $V_{DS} < V_{GS} - V_{TN}$ $I_D = K_n\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$	$\lvert V_{GS}\rvert \ge \lvert V_{TP}\rvert$ and $\lvert V_{DS}\rvert < \lvert V_{GS}\rvert - \lvert V_{TP}\rvert$ $I_D = K_p\left(\lvert V_{GS}\rvert - \lvert V_{TP}\rvert - \frac{\lvert V_{DS}\rvert}{2}\right)\lvert V_{DS}\rvert$
Saturation	$V_{GS} \ge V_{TN}$ and $V_{DS} \ge V_{GS} - V_{TN}$ $I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2$	$\lvert V_{GS}\rvert \ge \lvert V_{TP}\rvert$ and $\lvert V_{DS}\rvert \ge \lvert V_{GS}\rvert - \lvert V_{TP}\rvert$ $I_D = \frac{K_p}{2}(\lvert V_{GS}\rvert - \lvert V_{TP}\rvert)^2$

$v_{ic} = \frac{v_1 + v_2}{2}$ $v_{id} = v_1 - v_2$

$CMRR = \left|\frac{A_{dm-se}}{A_{cm-se}}\right| = \frac{\frac{g_m R_D}{2}}{\frac{R_D}{2R_{SS}}} = g_m R_{SS}$



$R_L' = r_0 \| R_D \| R_L$

Overall voltage gain from source v_i to output voltage v_o across R_L is:

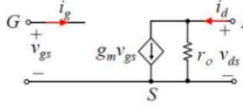
$A_v = \frac{v_o}{v_i} = \frac{v_o}{v_g} \times \frac{v_g}{v_i} = A_{vt} \times \frac{v_g}{v_i}$

$= -g_m R_L' \left(\frac{R_G}{R_I + R_G}\right)$

Terminal voltage gain between gate and drain is:

$A_{vt} = \frac{v_d}{v_g} = \frac{-g_m v_{gs} R_L'}{v_{gs}} = -g_m R_L'$

AC analysis: Small signal MOS model



- Since gate is insulated from channel by gate-oxide, input resistance = ∞.
- Small-signal parameters are controlled by the Q-point.
- MOSFET transconductance is geometry dependent.

$i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})$

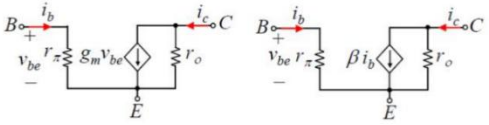
$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q-pt} = K_n(V_{GS} - V_{TN})(1 + \lambda V_{DS})$

where $K_n = \mu_n C_{OX}\left(\frac{W}{L}\right)$

$g_m = \frac{I_D}{\frac{V_{GS} - V_{TN}}{2}} \approx \sqrt{2K_n I_D}$

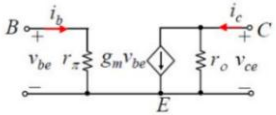
$r_o = \frac{\frac{1}{\lambda} + V_{DS}}{I_D} \approx \frac{1}{\lambda I_D}$ if $\frac{1}{\lambda} \gg V_{DS}$

Voltage-controlled current source $g_m v_{be}$ can be transformed into current-controlled current source.



$v_{be} = i_b r_\pi$
$g_m v_{be} = g_m i_b r_\pi = \beta i_b$
$i_c = \beta i_b + \frac{v_{ce}}{r_o} \approx \beta i_b$

Basic relationship $i_c = \beta i_b$ is useful for both dc and ac analysis when BJT is in forward-active region.



- This hybrid-pi small-signal model is the intrinsic low-frequency representation of the BJT.
- Small-signal parameters are controlled by the Q-point and are independent of geometry of BJT.

Transconductance:

$g_m = \frac{I_C}{V_T} \approx 40 I_C$

where $V_T = \frac{kT}{q} \approx 25\ \text{mV@25°C}$

Input resistance:

$r_\pi = \frac{\beta}{g_m}$

Output resistance:

$r_o = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C}$ if $V_A \gg V_{CE}$

$P_{av} = \frac{1}{T}\int_0^T \hat{i}_{out}\hat{v}_{out}\sin^2 2\pi f t\, dt$

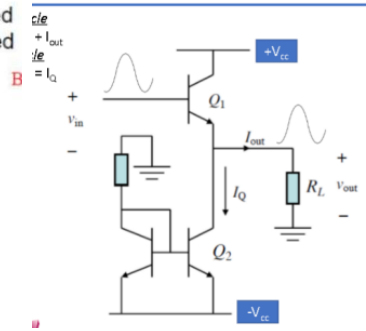
$= \frac{1}{2\pi}\int_0^{2\pi} \hat{i}_{out}\hat{v}_{out}\sin^2\theta\, d\theta$

$= \frac{1}{2}\hat{i}_{out}\hat{v}_{out}$

re clipping, $I_Q = \hat{i}_{out}$ and $\hat{v}_{out} = V_{cc} - V_{CE(sat)}$

$P_{out,max} = \frac{1}{2} I_Q (V_{cc} - V_{CE(sat)}) \approx \frac{1}{2} I_Q V_{cc}$

Emitter Follower: Large Signal Analysis



For Q_1: $\begin{cases} v_{in} = v_{be1} + v_{out} \\ v_{be1} = \frac{kT}{q}\ln\frac{I_{c1}}{I_{s1}} \end{cases}$ if Q_1 is active.

Also,

$I_{c1} = I_Q + \frac{v_{out}}{R_L} = I_Q + I_{out}$ if Q_2 is active.

Hence,

$v_{in} = \frac{kT}{q}\ln\left(\frac{I_Q + I_{out}}{I_{s1}}\right) + v_{out}$

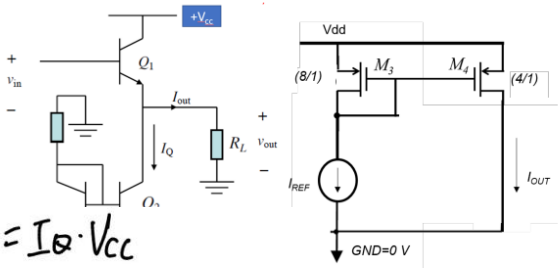
Weak nonlinearity

2. Consider the circuit of a class-A power amplifier in Fig. 2(a) with +Vcc = 10V, -Vcc = 0V.
(a) If the DC power drawn from the supply is 200 mW, what is the value of I_Q?
(b) If R_L = 200 Ω, what is the lowest possible value of V_{out} in this circuit (which will also determine the largest possible output sinusoid)?
(c) What is a problem with Class A power amplifier that is solved by Class B power amplifier? Explain in details.

(30 marks)

3. Figure 2(b) shows a PMOS based current mirror. The (W/L) of the Mosfets M3 and M4 are as shown in the figure. The parameters of the MOS are Kp'=30 uA/V², $|V_{TP}|$ = 0.5 V, and Early effect parameter λ=0.05. If Vdd = 8V, I_{ref} = 300 uA, answer the following questions:
(i) Find the value of Mirror ratio (I_{out} / I_{REF}) and I_{out}.
(ii) What is the % error introduced due to Early effect compared to the ideal case without Early effect?

(30 marks)



(i) $P_{DC} = I_Q \cdot V_{CC}$

$I_Q = 20\text{mA}$

(ii) $V_{out,min} = -I_Q R_L$

When Q1 entirely shuts off because Vin is at a very low voltage

$\therefore V_{out,min} = -4$

$MR = \frac{(W/L)_4}{(W/L)_3}\frac{(1+\lambda|V_{DS4}|)}{(1+\lambda|V_{DS3}|)}$

$|V_{DS3}| = |V_{GS}| = |V_{TP}| + \sqrt{\frac{2I_{ref}}{K_p'(W/L)_3}}$

$= 2.08\text{V}$

$MR = 0.64$ $I_{out} = I_{REF} \times MR = 192\mu\text{A}$

$I_{out,ideal} = 150\mu\text{A}$ (4/8 × Iref)

$\therefore$ error = 42μA

$\text{error}\% = \frac{\text{error}}{|\text{Iout,ideal}|} = \frac{42}{150} \times 100\% = 28\%$

$I_D = I_{D1} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TN})^2(1 + \lambda V_{DS1})$